UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,362	04/29/2004	David J. Hathaway	BUR920040074US1	3361

29625 7590 07/14/2005

MCGUIRE WOODS LLP
1750 TYSONS BLVD.
SUITE 1800
MCLEAN, VA 22102-4215

EXAMINER
LE, TOAN M

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,362	HATHAWAY ET AL.	
	Examiner	Art Unit	
	Toan M. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,12-19,25-28 and 30* is/are rejected.

7)☒ Claim(s) *7-11,20-24 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-6, 12-19, 25-28, and 30 are rejected under 35 U.S.C. 102(a) as being anticipated by "Statistical Delay Computation Considering Spatial Correlation", Agarwal et al. (referred hereafter Agarwal et al.).

Referring to claims 1 and 14, Agarwal et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), comprising:

determining at least one location information for one or more inputs to a timing test (page 274, section 4: 1st, 2nd, and 3rd paragraphs; page 275, 1st col., lines 3-10; equations 16-18); and

computing a timing slack for the timing test using the at least one location information (page 275, 1st col., lines 3-26; equations 19-22).

As to claims 2 and 15, Agarwal et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein the input to a timing test is a path or a logic cone (page 275, 1st col., lines 27-28).

Referring to claims 3 and 16, Agarwal et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a

circuit (Abstract), wherein the at least one location information comprises a bounding region for the one or more inputs to the timing test (page 274, 1st col., last paragraph; figure 1).

As to claims 4 and 17, Agarwal et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein said determining comprises defining the bounding region based an the locations of the one or more inputs to the timing test (page 274, 2nd col., 1st paragraph; figure 1).

Referring to claims 5 and 18, Agarwal et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein said determining further comprises modifying a. size of the bounding region to account for variations in delay among the one or more inputs to the timing test (page 274, 2nd col., 2nd and last paragraphs; figure 1).

As to claims 6 and 19, Agarwal et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein said computing comprises:

determining a slack variation factor based an the size of the bounding region (page 275, 1st col., lines 3-26; equations 19-21); and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test (page 275, 1st col., lines 27-28; page 274, 1st col., lines 1-12; equations 12-14).

Referring to claims 12 and 25, Agarwal et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein the at least one location information comprises an abstract location information (page 274, 1st col., last paragraph to 2nd col., 1st paragraph).

As to claims 13 and 26, Agarwal et al. disclose a method and a computer-readable medium containing instructions that, when executed, cause a computer analyzing the timing of a circuit (Abstract), wherein the abstract location information is based upon correlation of delay functions (page 274, 2nd col., 2nd paragraph).

Referring to claim 27, Agarwal et al. disclose a method a method of analyzing the timing of an integrated circuit (Abstract), comprising:

identifying an early path and a late path in the integrated circuit (page 274, 1st col., last paragraph);

determining a timing slack variation in the early path using location information an one or more elements i n the early path (page 275, 1st col., lines 3-26; equations 19-22);

determining a timing slack variation in the late path using location information an one or more elements in the late path (page 275, 1st col., lines 3-26; equations 19-22); and

computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path (page 275, 1st col., lines 27-28; page 274, 1st col., lines 1-12).

As to claim 28, Agarwal et al. disclose a method a method of analyzing the timing of an integrated circuit (Abstract), wherein the location information an the one or more elements in the early path and the location information an the one or more elements in the late path comprise bounding regions defined around the one or more elements in the early path and the one or more elements in the late path, respectively (figure 1).

Referring to claim 30, Agarwal et al. disclose a method a method of analyzing the timing of an integrated circuit (Abstract), wherein the method is performed for an early mode timing

analysis of the integrated circuit and a late mode timing analysis of the integrated circuit (page 275, 1st col., lines 3-26).

Allowable Subject Matter

Claims 7-11, 20-24, and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of the claims 7-9 and 20-22 is the inclusion of at least one location information comprising a centroid of the one or more inputs to the timing test, wherein the centroid having an average location and delay-weighted averaged location.

The reason for allowance of the claims 10-11 and 23-24 is the inclusion of calculating a first/second centroid to determine a distance between the first and second centroid so that a slack variation factor can be determined.

Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of the claim 29 is the inclusion of centroids calculated by considering the one or more elements in the early/late path.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"False-Path-Aware Statistical Timing Analysis and Efficient Path Selection for Delay Testing and Timing Validation", Liou et al., DAC 2002, Pages 566-569

"Statistical Timing Analysis Considering Spatial Correlations Using a Single Pert-Like Traversal", Chang et al., ICCAD 2003, Pages 621-625

"Modeling, Testing, and Analysis for Delay Defects and Noise Effects in Deep Submicron Devices", Liou et al., IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 22, No. 6, June 2003, Pages 756-769

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

July 7, 2005

MICHAEL NGHIEM
PRIMARY EXAMINER